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| 09/849,162 | 05/04/2001 | David E. Zeidler | 80113-0122 (D2382) | 9802 |

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| EXAMINER | |
|---|---|
| TRAN, TRANG U | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2614 | 4 |

DATE MAILED: 02/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/849,162 | ZEIDLER ET AL. | |
| | Examiner | Art Unit | |
| | Trang U. Tran | 2614 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9,20-23 and 26-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,20-23,26-31,34-38 and 41* is/are rejected.

7)☒ Claim(s) *6-9,32,33,39 and 40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1-9 and 20-23 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 9 and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Honma (US Patent No. 5,923,220).

In considering claim 1, Honma discloses all the claimed subject matter, note 1) the claimed an oscillator that generates the clock signal is met by the oscillator 1 (Fig. 3, col. 10, lines 12-27), 2) the claimed a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal, wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock is met by the controller 4 which calculates the frequency difference 102 and the receiving interval information 103 and to output a control signal 104 to control the oscillator 1 (Fig. 3, col. 9, line 55 to col. 10, line 43), and 3) the claimed a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range, wherein the incoming video signal is a

digital signal and the clock signal portion of the incoming video is program clock reference data for the digital signal is met by the variable range of a control signal 104 is limited within the range of the above mentioned frequency drift and the clock reproduction is continued (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64).

In considering claim 2, the claimed wherein the frequency range bounder includes an output multiplexer and a threshold register that stores at least one threshold value and that is coupled to the output multiplexer, wherein the output multiplexer receives a control signal and outputs one of the control signal and said at least one threshold value as a bounded control signal to limit the frequency of the oscillator to the selected range is met by the step S11, the maximum value of the obtained variable range is compared with the control information obtained in step S5 (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64).

In considering claim 3, the claimed wherein said at least one threshold register that stores at least one threshold value is a high limit register that stores an upper value and a low limit register that stores a lower value is met by the step S11, the maximum value of the obtained variable range is compared with the control information obtained in step S5 (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64).

In considering claim 9, the claimed further comprising a drive circuit that receives the bounded control signal and that drives the oscillator in accordance with the bounded control signal is met by the variable range of a control signal 104 is limited the oscillator 1 within the range of the above mentioned frequency drift and the clock reproduction is continued (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64).

Claim 20 is rejected for the same reason as discussed in claim 1.

In considering claim 21, the claimed further comprising the step of outputting a bounded control signal from the frequency range bounder to the oscillator to conduct the limiting step is met by the step S11, the maximum value of the obtained variable range is compared with the control information obtained in step S5 (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4-5, 22-23, 26-31, 34-38 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Honma (US Patent No. 5,923,220).

In considering claim 4, Honma discloses all the claimed subject matter, note 1) the claimed wherein the frequency range bounder includes an output multiplexer that selects one of the upper value, the control signal, and the lower value as the bounded control signal and outputs the bounded control signal to the oscillator to bound the oscillator frequency between an upper level and a lower level is met by the step S11, the maximum value of the obtained variable range is compared with the control information obtained in step S5 (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64). However, Honma explicitly does not disclose the claimed an output multiplexer that selects one of the lower value as the bounded control signal. The capability of an output

multiplexer that selects one of the lower value as the bounded control signal is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known an output multiplexer that selects one of the lower value as the bounded control signal into Honma's system in order to provide a clock reproducing device and the clock reproducing method in which the receiver design is facilitated by minimizing the difference between the received transmitting clock information and the reproduced clock information.

In considering claim 5, the claimed wherein the frequency range bounder includes at least one of a high comparator and a low comparator coupled to the output multiplexer, wherein the high comparator compares the control signal with a high limit and the low comparator compares the control signal with a low limit, and wherein the output multiplexer outputs the upper value as the bounded control signal if the control signal is above the high limit and outputs the lower value as the bounded control signal if the control signal is below the low limit is met by the step S11, the maximum value of the obtained variable range is compared with the control information obtained in step S5 (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64) of Honma.

Claims 22-23 are rejected for the same reason as discussed in claims 4-5, respectively.

In considering claim 26, Honma discloses all the claimed subject matter, note 1) the claimed a control logic circuit with a phase locked loop for receiving an incoming video signal and phase locking to a clock signal portion of the incoming video signal,

wherein the control logic circuit outputs a control signal for controlling an output of the oscillator based on the phase lock is met by the controller 4 which calculates the frequency difference 102 and the receiving interval information 103 and to output a control signal 104 to control the oscillator 1 (Fig. 3, col. 9, line 55 to col. 10, line 43), 2) the claimed a frequency range bounder in the phase locked loop that receives the control signal and outputs a bounded control signal that bounds the frequency of the oscillator to a selected range is met by the variable range of a control signal 104 is limited within the range of the above mentioned frequency drift and the clock reproduction is continued (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64), and 3) the claimed wherein said frequency range bounder is configured to generate a high limit signal and a low limit signal and then select one of said control signal, said high limit signal or said low limit signal for transmission to said oscillator depending on whether said control signal remains within pre-defined high and low limits is met by the step S11, the maximum value of the obtained variable range is compared with the control information obtained in step S5 (Figs. 3 and 7, col. 11, line 55 to col. 12, line 64).

However, Honma explicitly does not disclose the claimed an output multiplexer that selects one of the lower value as the bounded control signal.

The capability of an output that selects one of the lower limit signal as the bounded control signal is old and well known in the art. Therefore, the Official Notice is taken.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known an output that selects one of the lower

limit signal as the bounded control signal into Honma's system in order to provide a clock reproducing device and the clock reproducing method in which the receiver design is facilitated by minimizing the difference between the received transmitting clock information and the reproduced clock information.

Claim 27 is rejected for the same reason as discussed in claim 4.

In considering claim 28, Honma discloses all the limitations of the instant invention as discussed in claims 26 and 27 above, except for providing the claimed further comprising a high limit register for outputting said high limit signal and a low limit register for outputting said low limit signal. The capability of using the register for high or low limit signal is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using the register for high or low limit signal into Honma's system in order to synchronize the high limit signal with the phase locked loop.

Claim 29 is rejected for the same reason as discussed in claim 5.

In considering claim 30, Honma discloses all the limitations of the instant invention as discussed in claims 26 and 27 above, except for providing the claimed further comprising a low comparator for comparing said control signal and said low limit signal, wherein the output of said low comparator is provided to said multiplexer. The capability of using a low comparator for comparing said control signal and said low limit signal is old and well known in the art. Therefore, the Official Notice is taken. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the old and well known of using a low comparator for comparing said control

signal and said low limit signal into Honma's system in order to allow the phase locked loop operates in the desirable range.

Claim 31 is rejected for the same reason as discussed in claims 27-30.

Claims 34-37 are rejected for the same reason as discussed in claims 26-29, respectively.

Claim 38 is rejected for the same reason as discussed in claims 27 and 29-30.

Claim 41 is rejected for the same reason as discussed in claim 26.

***Allowable Subject Matter***

6. Claims 6-9, 32-33 and 39-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Trang U. Tran** whose telephone number is **(703) 305-0090.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John W. Miller,** can be reached at **(703) 305-4795.**

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

MICHAEL H. LEE
PRIMARY EXAMINER

TT TT
August 19, 2003